

REMARKS

1. Claims 19-25 are with the previous provisional election of claims 1-18 and 26-28.

2. Claim 26 is amended in response to the Examiner's objection and in response to the rejection of claim 26 under 35 U.S.C. 112.

3. Claims 1-3, 10-18, and 26-28 are rejected under 35 USC 103(a) as being unpatentable over the combination of U.S. Patents 6798241 (Bauer) and 6728901 (Rajski). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments distinguishing them over the cited references.

Claim 1

Claim 1 is best understood in relation to FIG. 4.

The "first multiplexer (62) receives the recited "input strobe signal" (STROBE) and the "first and second strobe signals" (CLKA and CLKB) and selects one of its input signals as the recited "first multiplexer output signal" (OSC) in response to selection control data (MODE_SEL).

The "first circuit" (54) responds to the OSC signal by generating the first and second strobe signals (CLKA and CLKB). Delay control data (DELAYA and DELAYB) supplied as input to first circuit 54 controls the delay between edges in the CLKA and CLKB signals.

The "control circuit" (everything else in FIG. 4 other than scan register 50) receives the first multiplexer output signal (OSC) and the input data (DELAY) specifying the delay between the edges in the CLKA and CLKB signals and produces the delay control data (DELAYA, DELAYB) and the selection control data (MODE_SEL).

The First Multiplexer

The Examiner correctly points out that Bauer's FIG. 5 shows a "first multiplexer" (520) controlled by "selection control data" (produced by device 25) for selecting from among several input signals to produce a "first multiplexer output signal" (DE). It is not, however, clear which of multiplexers 520 of FIG. 5 the Examiner considers to be the "first multiplexer".

The First Circuit

The Examiner correctly observes that Bauer does not teach the recited "first circuit" but incorrectly points to Rajski, FIG. 12 as teaching the recited first circuit.

The Examiner incorrectly refers to claim 1 as reciting a first circuit "wherein the generated signals are inputted back to the first multiplexer creating a linear feedback shift register (LFSR)" and then points to Rajski's FIG. 12 as disclosing a linear feedback shift register. However the following are apparent.

1. The recited "first circuit" is not a linear feedback shift register.
2. Nothing in claim 1 can be interpreted to be a linear feedback shift register or any kind of shift register.
3. Nothing in any of the applicant's drawings can be interpreted to be a linear feedback shift register.
4. Nothing in the applicant's specification mentions anything about a linear feedback shift register.
5. Rajski's FIG. 12, which shows a circuit under test 212 generating data 204 provided as serial input to a linear feedback shift register 206, does not meet the limitations of the recited "first circuit" of claim 1 which generates first and second strobe signals in response to the output of a multiplexer wherein edges of the first and second strobe signal are separated in time by a programmable delay set by delay control data. No such "first circuit" appears in Rajski's FIG. 12 or anywhere else in Rajski.

Thus Rajski and Bauer fail to teach the recited "first circuit"

The Control Circuit

The Examiner asserts that Bauer (cols 2-3) teaches the recited "control circuit". Note that as recited in claim 1

The control circuit inputs are:

- a. input data referencing a target delay, and
- b. output signal of the first multiplexer.

The control circuit outputs are:

- a. first selection control data to the first multiplexer
- b. delay control data supplied to the "first circuit."

Bauer's cols. 2-3 refer to Bauer's FIGs. 3, 4A, 4B, include a Summary of Bauer's invention, and include a portion of the "Brief Description of the Figures." Since the Examiner does not specify which parts of Bauer's col. 2 and 3 the Examiner believes disclose the recited "control circuit", the applicant will discuss all of cols. 2 and 3 in detail to determine whether anything in these two columns suggests the recited "control circuit".

Since Bauer's FIG. 3 shows an IC having a data input but does not receive the output of a multiplexer and does not produce selection control data or delay control data (or any apparent outputs), it does not appear that the Examiner is referring to Bauer's FIG. 3 as the recited "control circuit".

Since Bauer's FIGs. 4A and 4B are timing diagrams and not circuit diagrams, it does not appear that the Examiner is referring to Bauer's FIGs. 4A and 4B as the recited "control circuit".

Bauer's "Summary" section of cols. 2 and 3 talk generally about Bauer's invention which is to precisely align bits of IC signals to edges of a clock signal involving producing early, intermediate and late signals and in some way using the early and late signals to synchronize the intermediate signal with the clock signal. The only circuit discussed in the Summary section appears in col. 3, lines 19-28 relates to a sequence of flip-flops. The Summary does not discuss a "control circuit" as recited in claim 1 wherein

the control circuit inputs are:

- a. input data referencing a target delay, and
- b. output signal of the first multiplexer, and

the control circuit outputs are:

- a. first selection control data to the first multiplexer
- b. delay control data supplied to the "first circuit."

Thus Bauer's Summary fails to teach the "control circuit" recited in claim 1

The remaining portion of Bauer's col. 3 is a portion of "Brief Description of the Figures" covering Bauer's FIG. 1-11. Of those FIGs. only FIGs. 2, 3, 5, 6, 9, 10 and 11 show circuits. Since the Examiner considers one of multiplexers 520 of Bauer's FIG. 5 to be the "first multiplexer", and since claim 1 recites the "control circuit" receives the output data of the first multiplexer, then the applicant assumes that the Examiner is of the opinion that whatever receives the output of any one of multiplexers 520 of FIG. 5 is the recited "first control circuit". Note that the outputs of multiplexers 520 are received by a set of flip-flops 505, 509 and 513 which produce early, intermediate and late data signals DE, DI and DL. These flip-flops cannot alone be the recited "control circuit" because they do not have the recited "input data referencing a target delay," and do not produce as outputs the recited

- a. first selection control data to the first multiplexer(s) (520), or
- b. delay control data supplied to the "first circuit."

Perhaps the examiner includes more than just flip-flops 505, 509, and 513 in the "control circuit". The outputs DL, DI and DE are supplied to Window Adjustment Circuit 620 of FIG. 6 which produces control signals to devices 525 and 526 of FIG. 5 which control multiplexers 520. So if we include as the "control circuit", devices 505, 509, 513, 625, 525 and 526, that control circuit still lacks the recited "input data referencing a target delay" and fails to produce delay control data supplied to the recited "first circuit". Note that since the Examiner correctly points out that Bauer fails to teach the recited "first circuit", Bauer therefore cannot teach a "control circuit" that supplies delay control data to such a first circuit. Hence it appears Bauer and Rajski fail to teach the recited "control circuit" of claim 1. If the Examiner is of the opinion that Bauer teaches the recited "control circuit" the Examiner is respectfully requested to more specifically point out the particular elements of

Bauer's drawings that such a control circuit having the recited inputs and outputs.

It is believed, therefore, that claim 1 is patentable over the combination of Bauer and Rajski because while Bauer teaches the recited "first multiplexer, neither reference teaches either the recited "first circuit" or the recited "control circuit".

Claim 2

Claim 2 is patentable over Bauer and Rajski for reasons set forth above in connection with its parent claim 1. Claim 2 further recites that the control circuit carries out a calibration process wherein it sets the delay control data (DELAYA and DELAYB) so that the programmable delay between corresponding edges of the first and second strobe signals (CLKA and CLKB) matches a target delay (DELAY) referenced by the input data.

The Examiner cites BAUER col. 2 and 3 as teaching such a control circuit. The applicant assumes the Examiner is referring to Bauer's summary of the invention appearing in col. 2 and 3, and not the other material appearing in columns 2 and 3, and that the Examiner is of the opinion that the recited "control circuit" is somewhere to be found within Bauer's entire invention. Thus we look at Bauer's entire disclosure to determine whether it discloses a control circuit that sets the timing between Bauer's "first and second strobe signals" DI and DL

As can be seen from FIG. 5, the timing of each edge of the DL signal relative to a corresponding edge of the DI signal is controlled by multiplexer 520 of block 515 in response to the output of counter 526. Counter 526 is controlled by signals W_U/Db and W_{CE}. The device that controls those signals, and therefore the delay between DI and DL, is one of the window adjustment circuits 620 of FIG. 6. Bauer's col. 7, lines 29-41 teach that window adjustment circuit 620 sets the period between first and second strobe signals DI and DE to a value P. Since claim 1 recites that the period between the first and second strobe signals is set to a target value indicated by input data to the control circuit, the question is whether window adjustment circuit 620 sets the value of P to match a "target delay" indicated by input data to window adjustment circuit 620. The answer to that question is clearly "no" since, as we can see from FIG. 6 that window

adjustment circuit 620 does not have a data input indicating a target delay. Moreover, Bauer (col. 7, lines 29-57) teaches that the delay P between edges of the DI and DE signals is set so that edges of DI coincide with edges of the CLK signal and edges of DE occur earlier than edges of the CLK signal.

Thus claim 2 is also patentable over Bauer because Bauer does not teach that the delay P is set to match a target delay indicated by input data but for other reasons.

Note that the above argument appeared in the applicant's response to the previous office action and that the Examiner has repeated his argument for rejection while failing to rebut the applicant's argument against rejection. The Examiner is respectfully requested to rebut the above argument should the Examiner continue to reject under similar grounds.

Claim 3

Claim 3 depends on claim 2 and is patentable over Bauer and Rajski for similar reasons. Claim 3 is also patentable over Bauer because it recites "measuring a period of the first multiplexer output signal". The Examiner cites Bauer cols. 2 and 3 and FIG. 7C and 13A as teaching this, however no discussion of a calibration process involving measuring a period of any signal is found in any section or drawing of Bauer.

Note that the above argument appeared in the applicant's response to the previous office action and that the Examiner has repeated his argument for rejection while failing to rebut the applicant's argument against rejection. The Examiner is respectfully requested to rebut the above argument should the Examiner continue to reject under similar grounds.

Claims 10-14, 16 and 17

Claims 10 -14 depend on claim 1 and are patentable over Bauer and Rajski for similar reasons.

Claims 15 and 18

Claims 15 and 18 depend on claim 1 and are patentable over Bauer for similar reasons. Claim 15 further recites a "first capacitor having an adjustable first capacitance" and that the delay control

data controls the first capacitance". Claim 18 recites a "variable capacitor." The Examiner cites col. 5, lines 1 and 2 and col. 12, lines 45-48 of Bauer as disclosing an adjustable first capacitor or a variable capacitor, but no discussion of an adjustable capacitance or a variable capacitor appears in those sections of Bauer or in any other section of drawing of Bauer.

Note that the above argument appeared in the applicant's response to the previous office action and that the Examiner has repeated his argument for rejection while failing to rebut the applicant's argument against rejection. The Examiner is respectfully requested to rebut the above argument should the Examiner continue to reject under similar grounds.

Claim 26

Claim 26, best understood with reference to the applicant's FIG. 5, recites an apparatus comprising;

means (80) for generating an edge of the first strobe signal in delayed response to each edge of the input strobe signal;

a first multiplexer (62) for receiving the input strobe signal (STROBE) and the second strobe signal (CLKB) and for providing either one of the input and second strobe signals selected by first selection control data (MODE_SEL) as a first multiplexer output signal (OSC);

a tapped delay line (57) comprising a plurality of gates (56) connected in series for receiving the first multiplexer output signal (OSC) and producing an edge in a separate tap signal at an output of each gate in delayed response to each edge in the first multiplexer output signal (OSC), wherein a signal delay through each gate is a function of voltage supplied to the gates (see FIG. 5, output of device 102);

means (102) for adjusting the voltage supplied to the gates in response to delay control data (DELAYB);

means (59, 61) for receiving the tap signal produced by each gate as input, for selecting one of the tap signals as a selected tap signal in response to the delay control data (DELAYB) and for generating an edge in the second strobe signal (CLKB) in response to each edge in the selected tap signal; and

a control circuit (not shown in FIG. 5, but similar to that of FIG. 4) receiving the input data and the first multiplexer output signal (OSC) for supplying the first selection control data (MODE_SEL) to the first multiplexer and for supplying the delay control data (DELAYB) to the first circuit, wherein the first selection control data and the delay control data are functions of the input data.

The Examiner cites the multiplexer 520 of Bauer's FIG. 5 as being similar to the recited "first multiplexer". Since there are three multiplexers 520 in Bauer's FIG. 5, the Applicant assumes the Examiner is referring to the leftmost multiplexer 520. This multiplexer 520 produces a "first multiplexer output signal" DE.

The Examiner cites Bauer's FIGs. 5 and 7C-7E as disclosing the recited "means for generating ... the first strobe signal". Since FIGs. 7C-7D are timing diagrams, it is unclear as to how these disclose means for generating a signal. If the Examiner is referring to the circuit of FIG. 5 in its entirety as the recited "means for generating ... the first strobe signals, then since the circuit of FIG. 5 generates four output signals AI_0 , DL_0 , DI_0 and DE_0 , it is unclear as to which of these four signals the Examiner considers to be the "first strobe signal". On the other hand, since the Examiner cites particular portions of Bauer's FIG. 5 as being other elements of claim 1, it seems more reasonable to conclude that the Examiner is of the opinion that only a particular portion of Bauer's FIG. 5 is the recited "means for generating ... the first strobe signal." If that is the case, then it is unclear as to which portion of FIG. 5 the Examiner considers to be that means and which of the many signals of FIG. 5, the Examiner considers to be the "first strobe signal". However if we consider the leftmost multiplexer 520 to be the recited "first multiplexer", then we can consider any one of the output signals of the leftmost tapped delay line of FIG. 5 to be the "first strobe" signal. In that case we can consider the leftmost tapped delay line of FIG. 5 to be the recited "means for generating... the first strobe signal" and can consider the signal D0 to be the recited "input strobe signal".

The Examiner cites Bauer col. 5, lines 1-2 and FIG. 5 as disclosing tapped delay lines, and indeed we see a tapped delay line at the input of each multiplexer 520 of FIG. 5. The question is which tapped delay line the Examiner concludes is the recited tapped delay line. Since claim 1 recites that the tapped delay line receives the

"first multiplexer output signal, and since we have assumed the Examiner is referring to the leftmost multiplexer 520 as the recited "first multiplexer", then we can also assume the tapped delay line at the input of the middle multiplexer 520 is the recited "tapped delay line".

The Examiner cites Bauer's col. 2, 3 and 12 as disclosing the recited "means for adjusting" the supply voltage of the gates of the first tapped delay line. Applicant assumes that the Examiner refers to Bauer's Summary section in col. 2 and 3 as discussing adjusting the supply voltage of the gates of a tapped delay line of FIG. 5. The Applicant has carefully reviewed Bauer's Summary section and col. 12 and has been unable to find a discussion of any means for adjusting the power supply voltage of the gates of a tapped delay line of FIG. 5. Thus it appears that Bauer fails to teach the recited "means for adjusting".

The Examiner again cites an unspecified one of the multiplexers 520 of Bauer's FIG. 5 as being the recited "means for receiving the tap signal produced by each gate and ... generating the second strobe signal". Since we have assumed the Examiner refers to the middlemost delay line of FIG. 5 is the recited "tapped delay line", it is reasonable to assume that the Examiner is referring to the middlemost multiplexer 520 is the recited "means for receiving the tap signal produced by each gate" of that delay line. Thus we assume that the DI output signal of that multiplexer 50 is the recited "second strobe signal". But now a problem arises in that the "second strobe signal" (DI) output of that "means for receiving" is not supplied as input to the leftmost multiplexer 520, which we have assumed is the "first multiplexer". Therefore, while FIG. 5 shows the recited "first multiplexer" and the recited "means for ... generating the second strobe signal", the two elements are not interconnected in the manner recited in claim 1.

Thus the claim 26 is patentable over Bauer because Bauer fails to disclose the recited "means for adjusting" and fails to teach that the "second strobe signals" (DI) should be supplied as an input to the "first multiplexer" (leftmost multiplexer 520.

Note that the above argument appeared in the applicant's response to the previous office action and that the Examiner has

repeated his argument for rejection while failing to rebut the applicant's argument against rejection. The Examiner is respectfully requested to rebut the above argument should the Examiner continue to reject under similar grounds.

Claims 27 and 28

Claims 27 and 28 depend on claim 26 and are patentable over Bauer for similar reasons and for reasons similar to those discussed above in connection with claim 2 and 3, respectively.

4. Claims 4-9 are rejected under 35 USC 103(a) as being unpatentable over the combination of Bauer, Rajski and U.S. patent 6058496 (Gillis). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments distinguishing them over the cited references.

Claim 4

Claim 4 depends on claim 2, and the Examiner cites Bauer and Rajski as teaching the limitations of parent claim 2. and cites Gillis only as teaching the additional limitations of claim 4. Claim 4 is patentable over the combination of Bauer, Rajski and Gillis since, for reasons discussed above in connection with claim 2, Bauer and Rajski fail to teach all of the limitations of claim 2.

The Examiner cites Gillis as teaching a calibration process including determining a difference between a number of edges of a number of edges of a reference clock signal occurring during a first period determined by counting a predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer providing the first strobe signal as the first multiplexer output signal, and a number of edges of a reference clock signal occurring during a second period determined by counting the predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer providing the second strobe signal as the first multiplexer output signal.

Though not directly stated in claim 4, that difference is a measure of the period or frequency of the first multiplexer output signal (OSC) of the applicant's FIG. 4 when the first multiplexer is

configured to select the first or second strobe signal, thereby causing the OSC signal to oscillate periodically. Although Gillis may teach a method for measuring a signal period or frequency, it would not be obvious for one of skill in the art to incorporate into Bauer's circuits additional circuitry using any technique for measuring the frequency or period of Bauer's "first multiplexer output signal" (DE) since the DE signal, being a delayed version of the D₀ signal (a single line of a data bus) is not periodic and therefore has no measurable period or frequency. Also Bauer does not provide any discussion as to why such a calibration process might be of any benefit even if the DE signal were somehow rendered periodic. Measuring the period or frequency of the DE signal or any other signal of Bauer's circuit would provide no benefit in the context of Bauer's application.

Claim 4 is therefore patentable over the combination of Bauer, Rajski and Gillis.

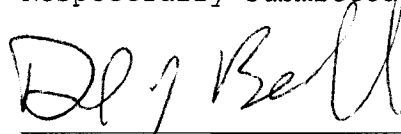
Note that the above argument with respect to the teachings of Gills appeared in the applicant's response to the previous office action and that the Examiner has repeated his argument for rejection while failing to rebut the applicant's argument against rejection. The Examiner is respectfully requested to rebut the above argument should the Examiner continue to reject under similar grounds.

Claims 5-9

Claim 5 depend on claim 4 and are patentable over the combination of Bauer, Rajski and Gillis for similar reasons.

In view of the foregoing amendments and remarks, it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

A handwritten signature in dark ink, appearing to read "D. J. Bedell", written over a horizontal line.

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